ELECTRICAL ENGINEERING DESIGN-BUILD PROJECT: CLASS-D AUDIO AMPLIFIER DESIGN AND CHARACTERIZATION

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ABSTRACT

This paper describes the design, implementation and results of the second year Basic Engineering Project subject performed by the students of Electronic Engineering degree (EE) and Audiovisual Systems Engineering degree (AV) at Telecom-BCN. Two groups of twenty students complete it every semester working in teams of four members. The students are asked to fulfill the design, implementation and verification of a given block of a product specified by the faculty. The product in the last three years, with small variations every year, has been a campus-wide audio announcements distribution system using wireless communications. All students know the requirements and specifications of the whole product and of the interfaces between blocks and the students of each degree are assigned to design, implement and test only one of the blocks.

The EE students' assignment is a 2 W class-D audio amplifier, with a given bandwidth, power efficiency and harmonic distortion. The AV students should design, implement and verify a virtual instrument to characterize and test the performance of the audio amplifier and to correct its frequency response by digital signal processing. This subsystem is developed in Matlab and uses the computer audio card to generate the test signals and record the amplifier output. They all develop the product documentation following our adaptation of the LIPS methodology.

The pedagogical aspects of this subject were already presented in a previous CDIO Conference (at DTU in 2011). In this paper, the design-build projects performed by the EE and AV students, which complement each other and are integrated at the end of the semester, are presented as Learning Objects, with enough detail to allow other institutions considering its implementation. Additionally to the practical aspects (design guidelines, complexity, components and tools, cost…), the learning outcomes and students achievements are also presented. Also the dos and don'ts derived from the experience of three and half years of implementation.

KEYWORDS

Design-Build Project, Electrical Engineering, Standards: 5, 11

INTRODUCTION: THE DESIGN-BUILD SUBJECTS PATH AT TELECOM-BCN

Four design-build project subjects are distributed along the curricula of each of the five bachelor degrees taught at Telecom BCN, the Electrical Engineering School of Universitat Politècnica de Catalunya (UPC), in Barcelona, Spain. Their design and first-time implementation and results were described in previous CDIO Conference communications. The first year has an Introduction to Engineering course (Bragós, 2010), (Pegueroles, 2013) which includes a partially guided project through a complex system, but with low technical difficulty. It has, however, a broad scope, given that the students start from a system-level client specifications, design parts of the system, build the whole system and should define a business idea based on a similar device. On the other hand, the second year project (Basic Engineering Project) (Bragós, 2011), has a higher technical difficulty and emphasizes the modular structure of complex ICT systems, although a work team will only develop one of the system blocks. In the third year project (Advanced Engineering Project) (Bragós, 2012), larger working groups should develop a whole system, including its business plan. They should conceive the product, define the project breakdown structure and work packages, distribute them between the sub-teams, design and implement the sub-systems, integrate them and define a business plan based on the product. The fourth and last year, the individual students join a research department or company to perform their degree thesis. All project subjects are located on the second half of each year although they are offered every semester to allocate the students with different progression.

THE BASIC ENGINEERING PROJECT SUBJECT

The Learning Objects we describe in this paper is included in the Basic Engineering Project, the second year project subject, which has six ECTS credits. Two credits are used to learn the contents and practical aspects on the regulation of telecommunications, which is required for the professional ICT engineering practitioners in Spain. The Basic Engineering Project is performed in the remaining 4 ECTS credits (3 hours/week in the lab + 4 hours/week of autonomous work). The students of electrical engineering are attending their second year, which is common to all of them, but they are going to split in four majors in the third year: electronics, audiovisual systems, computer networks and communication systems (see figure 1). There is also an additional degree, which has a wider scope, Telecom Science and Technology. Then, the students' interests can be slightly different.

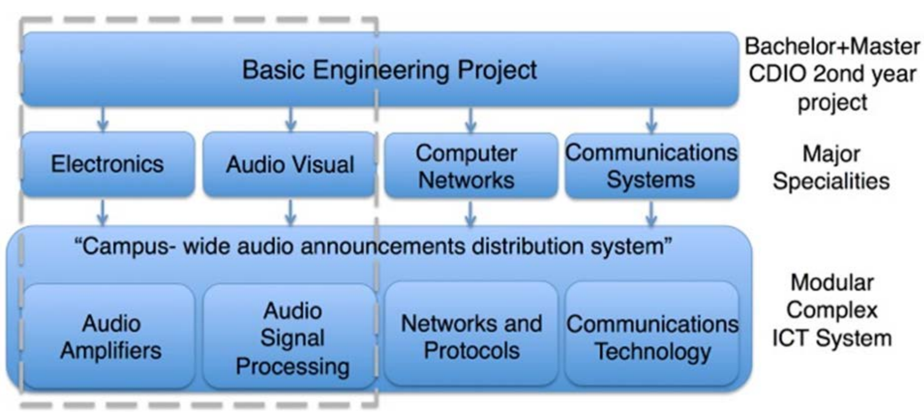

Figure 1. Modular complex ICT system: "Campus-wide audio announcements" The dashed block shows the parts of the Basic Engineering Project described in this paper.

The product proposed to be designed is divided in four or five blocks including aspects of hardware development, communications, network protocols and audio/image/video signal processing. The product in the last three years, with small variations every year, has been a campus-wide announcements distribution system using wireless communications (Figure 2). All students know the requirements and specifications of the whole product and of the interfaces between blocks and the students of each degree are assigned to design, implement and test only one of the blocks. The subject is performed simultaneously in several labs, with support of lecturers from different departments. This paper describes the projects developed in the labs corresponding to Electronic Engineering and Audiovisual Systems Engineering. There is a second paper describing, as Learning Objects, the projects corresponding to Computer Networks Engineering and to Communication Systems Engineering. The system is currently more complex, including video codification and distribution and data-stream control through an Android app, but we will describe a reduced version for sake of simplicity.

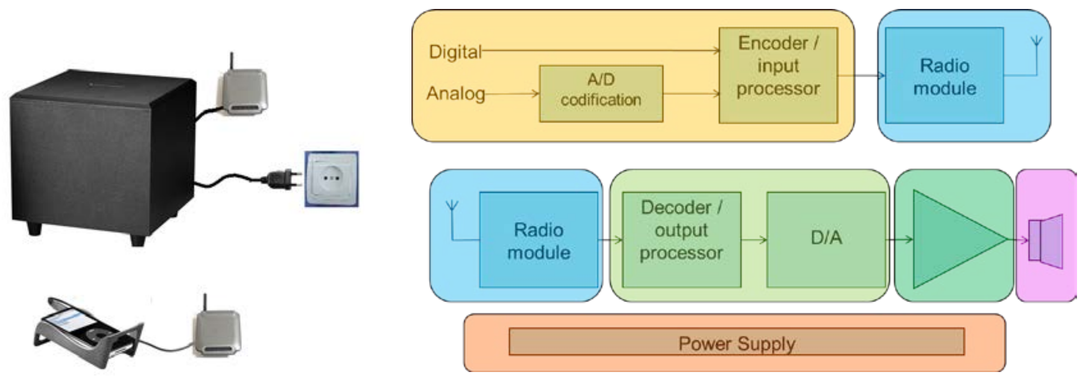

Figure 2. Campus-wide audio announcements distribution system using wireless communications and system division in blocks. Each block is performed by a student's team.

Course goals and learning outcomes

Course goals:

- Consolidation and improvement of the learning outcomes of previous and simultaneous courses
- Enhancement of the 4th group of CDIO skills at medium level (mainly Design and Implementation related skills)
- Acquisition of personal (CDIO Syllabus group 2) and interpersonal (CDIO Syllabus group 3) skills at medium level.

Learning outcomes:

- Project management and documentation skills
- Specific discipline-related knowledge about the project topic
- Practical design and implementation skills
  - System and circuit level simulation and characterization
  - Complex systems programming in a high level language (Matlab)
  - Measurement strategies
  - Electronic components selection and circuit building
- Generic skills learning outcomes (assigned and defined in the degree syllabus)

Course design

The students are grouped in teams of 4-6 (depending on the project complexity) and sign a team constitution agreement in which they define their role and commit to have a common ambition of reaching a given mark (pass, good, outstanding). The generic course schedule is shown in the following table.

Table 1
Generic course schedule

Week	Activity	Deliverables
1	- Course introduction - Brainstroming about the product structure and specs. - Puzzle assignment	
2-3	- Puzzle activities about disciplinary contents referred to the project - Block requirements definition	1-2 pages report + 2 slides on each puzzle topic
4	- 3d puzzle about block implementation alternatives - Brainstorming about tasks and work packages planning	Requirement Specification document
5 -8	- Block design and prototyping	Project Plan document Prototype characterization
9-12	- Block improvement and finishing. Integration.	Second prototype design
13	- Final project presentation	Project final report

The documentation has been adapted from the LIPS standard [3]. Four documents are required: Requirements & Specifications, Project Plan, Progress Reports and Final Report.

Course assessment

The initial individual assignments have a small weight in the mark but it is mandatory to deliver them on time. There is a strong penalty (20% per delayed item) if less than 80% are delivered on time. Another 30% of the mark is obtained from tests about individual knowledge of the project. The remaining 60% of the mark is assigned to the whole team performance. Although this is a global team mark, there is a 20% modulation of the individual mark which comes from the team coherence and from the cross-assessment between the team members.

- Puzzle and project individual assignments.......................10%
  (20% penalty in the whole mark if less than 80% on time)
- Project …………………………………………………………60%
  - 20% half course performance
  - 40% final performance
- Project contents individual tests (2)……………………….30%

LEARNING OBJECT 1. CLASS-D AUDIO AMPLIFIER

Initial requirements and specifications

The EE students assignment is to design and build a 2 W audio amplifier, with a bandwidth of 20 Hz to 20 kHz, with a power efficiency better than 80% and a harmonic distortion better than 1% with budget restrictions. The Class-D amplifier as a project course theme has been previously used (Trullemans, 2008). The specifications are not given in that way the first day. Only the generic requirement of designing and building an efficient amplifier module suitable for the product described in the previous section is given at the beginning of the course. Along the first 2-3 sessions, the students are asked to look for the specifications by benchmarking similar products. At the end, the following specifications (Table 2) are presented

Table 2
Amplifier specifications

	Conditions	Symbol	Min	Typ	Max
Output Power	THD≤1%; RL=8Ω; f=1kHz	Po	1W	2W	3W
Energetic Efficency	at 1W; RL=8Ω	η	80%		
Frequency Response	Both ranges			100Hz-10kHz (+-1dB)	
	must be fulfilled			20Hz-20kHz (+-3dB)	
Total Harmonic Distorsion + Noise	at 1kHz	THD+N		1%	
Signal Noise Ratio	f=20Hz-20kHz; THD=1%	SNR	60dB	70dB	80dB
Estimated Cost	Materials only (prototype)				25 €
	Production (1000 units)				10 €
Goal: to achieve the given specifications.					
Once achieved, the best product is that which has the lower cost					

Contents of the first sessions, to acquire the background

The second year students have only attended an introduction to electronics course and a second course on analog electronic functions. They don't have a background on audio amplifiers. They acquire the basic concepts using the puzzle technique. The first day, they attend the course introduction, the product definition and a seminar on how to search for relevant information in Google and in technical and scientific databases (ieeexplore, Scopus…), and how to cite the information they found. They are asked to build the 4 people teams and to prepare each one a 1-2 pages report and 2 slides on an amplifier class (A, B, AB or D). Two references are given as seed resources (Soclof, 1991) and (E. Gaalaas, 2006). The second day, after the experts meeting, each team member presents to the others his amplifier class. This takes one and a half hours. At the end, there is a discussion and they come to the conclusion that the only one that can fulfill the system requirements is the class-D structure. The second half of the session is about project management and documentation. The second puzzle is about four aspects of Class-D amplifiers: architecture (PWM Modulation vs Δ-Σ), signal spectrum, output stage and output filter). They are also asked to find amplifier modules (not single chips but OEM modules) to perform a benchmarking. The third day, after performing the puzzle, and generating the specifications from the benchmarking, they are asked to perform a behavioral simulation of the Class-D structure. They are recommended to choose the PWM-Modulator structure instead of the Δ-Σ structure for sake of simplicity. They are given a seed Matlab script that performs the modelling and simulation of the basic features and are asked to check the effect of changes in several parameters and to complete the models.

At the end of the third day, they are asked to prepare the Requirements and Specifications document, which constitutes an agreement with the client. It includes a background section that is built by putting together the small reports each one has prepared for the puzzles. They should take care of the coherence of the different parts and cite the references properly.

Detailed schedule of the project

The specific schedule of the last semester implementation is included in the attached documentation. The three first sessions are fully scheduled, but after that, there are two blocks of 5-6 weeks in which the student teams have the freedom of distribute the tasks and the workforce to fulfill the project plan. The first block is devoted to design and build a functional prototype, mounted on a breadboard, which viability is discussed in the Critical design Review at week 9. In the second block, the students teams build an improved second prototype on a printed circuit board (pad array board or custom printed circuit board). At the end, the students characterize the amplifier with the virtual instruments developed by the AV student teams. The first three weeks, the students should present the materials prepared to fulfil the puzzles (individual assignments, tollgates 1 and 2) and the Requirements and Specifications document (tollgate 3). The 4th week, the project plan with the definition of tasks and a Gantt diagram and a preliminary proposal for the circuit architecture and critical parameters. There is a Preliminary Design Review (tollgate 4) that validates (or not) the viability of the proposal. The 9th week there is a meeting with the clients (lecturers acting as supervisors) to perform the Critical Design Review (Tollgate 5). The circuit prototype at that point is built on a breadboard, and displays several performance limitations due to the excessive resistance in connections and parasitic capacitances. The supervisors can, however, determine if the circuit is suitable and will meet the specifications when it is mounted on a printed circuit board. If not, variations in the structure or components are suggested. The last week, in a second review (The Final Design Review, tollgate 6), the student teams show the final performance, measured according to the protocol that has been proposed by the students and approved by the supervisors. This measurement protocol includes the use of the characterization tool performed by the AV students. The students have free access to the lab, but they are asked to do their lab work mainly during the three hours per week during which the faculties are there. This double role faculty/supervisor-client makes sometimes difficult to separate the roles, because the students make questions and ask for help about pitfalls in the circuit behaviour or measurement procedures the same way they do in a regular laboratory class. We tend to give more importance to the development of the project than to the performance of the circuit.

Materials which are provided

The first two years, we gave absolute freedom to the students to choose their circuit architecture and their components. This leaded to some solutions that could be unstable or that would never work correctly. Also obliged us to perform weekly acquisitions of components to the distributors (Farnell, Digikey, …). It has to be taken into account that the students are only on his 4th semester and may not have clear criteria for selecting components. In fact, is one of the learning outcomes of this project. We now give them a closed set of alternatives for each block of the circuit, some of them which are better and more expensive and some others which are more basic but cheaper. If a given team shows to be more creative, we allow them to ask for extra materials but we explicitly warn them that the system should work at the CDR tollgate.

Except those creative solutions, the chosen architecture for the amplifier is usually the PWM modulator followed by a full-bridge or a half-bridge and a second order LC filter (figure 3). The main degrees of freedom are the design of the triangular or sawtooth signal generator, their levels and frequency, the power supply (unipolar or bipolar and its value), the comparator (simple-double output) and if the output stage is a half or full bridge, which has implications on the power supply voltage needed and also on the complexity of the output filter. Choosing a symmetrical power supply drives to a simpler design but is not considered a good practice for a low power amplifier like this one. Then, they should add level shifters at different points in the circuit, which affects the low frequency response. The most conflictive part has shown to be the power bridge. If they implement it through a bridge driver and external transistors, they usually burn a lot of them due to a bad synchronization of transistor gates because of a bad design or a wrong connection. They have the power electronics subject after this one. So we propose them a given integrated circuit which implements a full bridge with its driver and that can be configured as two independent half-bridges. A finite set of low-Rs inductors and capacitors are proposed, so we can have them in stock. We also propose three possible alternatives for implementing the triangular or sawtooth wave generator: a dedicated chip, a realization with discrete opamps or a realization based on an astable multivibrator followed by an integrator. Given that the suitable frequency for the modulation is above 200 kHz, the selection of the operational amplifiers is not so trivial. About the passive components, they own a small set and they can ask for additional values to the lab responsible. Some of the active devices only exist in SMD format, so we provide adaptors to allow prototyping with them.

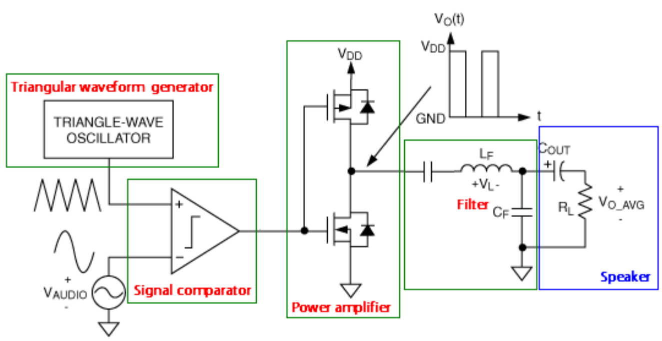

Figure 3. Block diagram of the usual amplifier architecture, a PWM modulator followed by a half or full transistors bridge (simplified in the figure) and a Second order LC filter.

Examples of results

The detailed schematics and results can be found in two examples of final reports that are attached. Following figures show two realizations, one using pad-array printed circuit board and a second one using custom printed circuit board. There is a CNC milling machine in the lab to perform the PCB prototypes. There are not explicit classes on PCB design and manufacturing. The students interested on that learn by themselves through tutorials and with the support of the laboratory staff. Although commercial CAD tools (Cadence) are available in the lab, open tools like Design Spark, available at RS webpage, are being promoted the last years in order to allow the students working at home with the layout design.

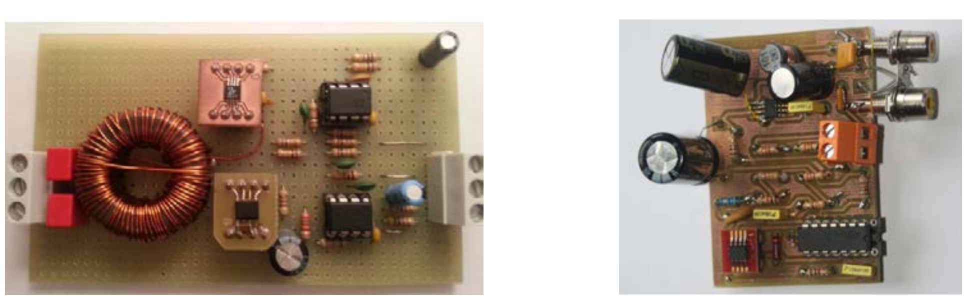

Figure 4. Two amplifier implementations, one using pad-array printed circuit board (left) and a second one using custom printed circuit board (right).

Student's achievements

Very few teams reach the fulfilment of all the specifications, the attached reports show an example. They usually reach the required bandwidth and typical power (1 W) and a power efficiency better that 70%, but the distortion is usually above the requirements. They are told at that point that most causes of these drawbacks are because of the discrete realization and the very simple structure. Amplifier modules in that range of power are based on single chip solutions, with costs below 1$ for the chip and below 4 $ for the module, but there are few design opportunities at circuit level when using these chips, and they understand that the project has been set-up under pedagogical conditions.

Students are motivated and use to engage with the team work with very few exceptions. There are several drop-off cases (2%) because they do not stand the pressure of the team assignments and usually leave the course after 3-4 weeks. They can repeat it in the following semester if they have enrolled a lower amount of credits. There are a few cases 2-3% of individual students failing the subject because their team did not perform very well and additionally, the peer-evaluation and the test-based assessment of their individual work showed a very low individual performance. All other cases use to have marks between 6,5 to 9,5 over 10, with a few very high marks (10) for a 2-5% of students with an exceptional performance. It has to be taken into account that the failure rate for regular subjects is around 30%.

Changes performed along the course realizations. Dos and Don'ts

Some of the performed changes have already been commented in the "materials which are provided" section. Along the time, we have selected a set of partial solutions for several circuit blocks in order to guarantee that a working circuit can be delivered in the CDR tollgate by most of the teams. This project is less guided that the first year one, and the students have the freedom of determining the tasks into the two six-weeks blocks, but in the first realizations of the course, the students showed a lack of ability in calculating the real amount of time and workforce to perform the tasks, so we added more contents in the weekly report. They are now asked to draw their real circuit at the end of every week session and to compare it with the foreseen project state. Then they realize the real progression of their design and distribute the workforce in a more coherent way.

List of additional resources

The document we give to the students with the suggested alternatives for the design of the blocks is added as an annex.

LEARNING OBJECT 2. D-CLASS AMPLIFIER SIMULATION AND VIRTUAL INSTRUMENTATION FOR TESTING AND IMPROVEMENT

Initial requirements and specifications

The AV students assignment is to elaborate the "Requirement and Specifications" and then, implement, test and verify three different packages of software tools:

- D-class simulator in time and frequency domain.
- The necessary virtual instruments to test the main parameters of the D-class amplifier.
- A digital audio equalizer with a minimum of 6 bands with a gain of +-3 dB.

The objectives behind each package are:

- Understand the details of how a highly non-linear electronic device can operate as a linear device, using and applying basic analog and digital signal processing concepts.
- In the second tool, the main objective is to understand some concepts of audio amplifiers and its characteristics as gain, frequency response and harmonic distortion and its different forms and strategies to measure.
- The objective of the equalizer is to illustrate the concept of pre-equalization and how some basic tools can enhance the final performances of operation of our initial design.

These are the summarized main tasks and the objectives that the instructor have in mind, but the student is not familiarized with D-class amplifiers or the main technical specifications or parameters of high quality audio amplifiers or how to measure in order to elaborate the "Requirement Specifications".

Contents of the first sessions, to acquire the background

The objective of the next following 2/3 sessions is that the students get an informal knowledge about the main type class of amplifiers (A, B, AB, D) and its main technical characteristics, what are the most important characteristics to measure in an audio amplifier and how can be measured (Bandwidth, distortion, efficiency, Power gain, ...). This two sessions are covered as puzzle sessions (as explained before), where each student of the group is assigned to a topic (a type of amplifier in the first puzzle, or characteristic to measure in audio amplifiers in the second) that they will have to explain in the next session to the rest of the group (with the assistance of two transparencies and a two pages text, that are the deliverable documents of the puzzle sessions).

With this background (at the end of third session), they can start to translate with their interpretation, the given "informal specification" into an initial Specifications Requirement document (a form is provided). This document includes a background section, which is filled by joining and integrating the documents prepared to fulfil the puzzle assignments, and taking care to correctly give and cite the references. In general this task requires more than one iteration because their difficulty to scope the globality of the project.

Detailed schedule of the project

Once validated the Requirement Specification, the groups are asked to present the project Plan Document, which includes a Time Plan and a Work Package description. The remaining project weeks, the groups are supposed to follow this plan that is checked at two points: the Preliminary Design Review (PDR), at week 7, when the first prototype should be working and the Critical Design Review (CDR), at week 11, when there is no return in the chosen alternatives and the second prototype should be working, and only finishing and improving activities should be running.

Materials which are provided

In the case of AV there are no special material needs with the exception of a few materials to implement passive RLC filters or diode based signal limiters to perform simple tests of the virtual instrumentation. All the tools will be programmed in a high level language (Matlab without Toolboxes or probably Python in the next future) using the basic audio I/O card of the computer system (Mac or PC) to generate the corresponding analog test signals and acquire the signals to analyze. We recommend at least one computer equipped with a high-end audio analog I/O board to illustrate and demonstrate the limits and effects of the converters precision and the different sampling rates.

Examples of results

In the following figures some final graphical results are shown, corresponding to each package assigned:

- D-class simulator in time and frequency domain (Figure 5).
- The virtual instruments to test the main parameters of the D-class amplifier (Figure 6).

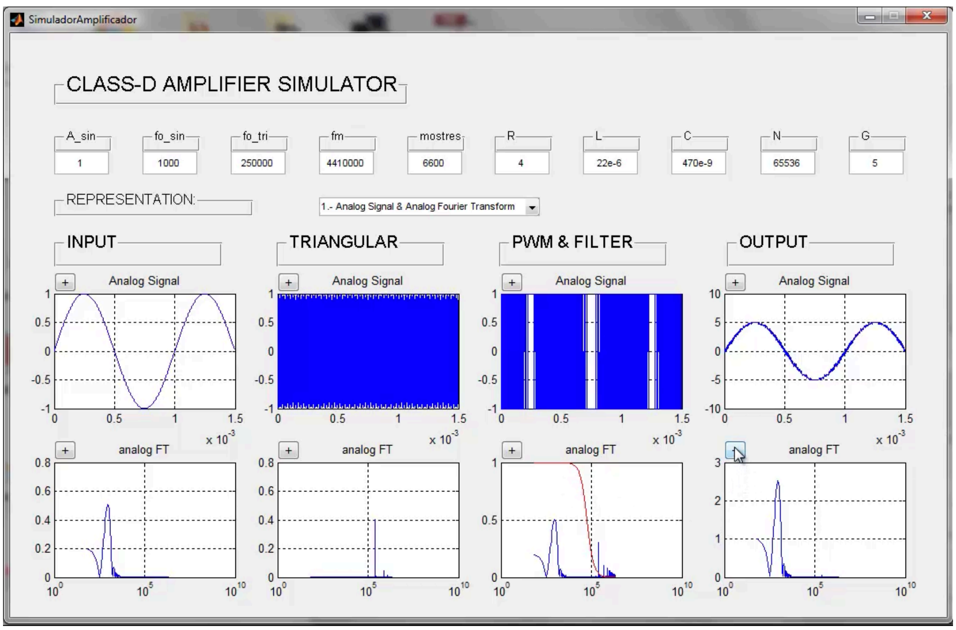

Figure 5. Global view of the D-class amplifier simulator where all relevant signals can be plotted individually (pressing on sign +) and it can be observed in time and frequency domain.

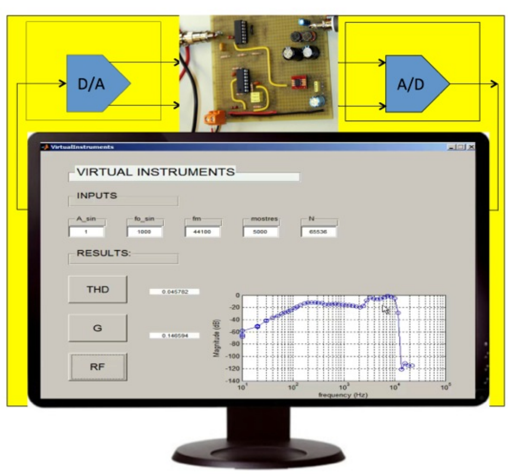

Figure 6. Display of the corresponding Virtual Instrument results (programmed in Matlab), that measures and plot the frequency response, harmonic distortion and voltage gain of a real prototype D-class amplifier connected to the audio card A/D and D/A converters.

Student's achievements

The particular achievements in the AV project with different degrees are:

- Consolidate the correct application of sampling and Nyquist theorems in the analogic a digital signals environment, basic spectral analysis and windowing, signal filtering and digital filters design.
- Introduce the idea of Complex Software system development and the need of Software Documentation. Documenting is boring but necessary.
- Working in Group: Project planning strategy and task division.

CONCLUSIONS

The second year Basic Engineering Project subject has reached a steady state after seven realizations, although improvements are added year by year. The need of providing partial guidance and restricting the degrees of freedom respect to the first implementations has been the more relevant change in the subject design. Reaching the final week with a non-working amplifier or software package generates frustration in the students, so we are doing o more strict control on the time plan real follow-up in order to ensure that a product will be ready at the end of the course. The performance of the product will be, of course, different among teams, and this gives the differences in the marks.

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